

What We Claim Is:

1. A transconductance power amplifier for amplifying a signal to a capacitive load, comprising:

a first N-channel enhancement MOSFET transistor operatively arranged to source current to said capacitive load, wherein said first N-channel MOSFET transistor has a threshold gate to source voltage;

a second N-channel enhancement MOSFET transistor operatively arranged to sink current to said capacitive load;

an operational amplifier operatively arranged to transmit and amplify an input signal to both of said first and second MOSFET transistors; and,

means for biasing said first N-channel enhancement MOSFET transistor such that its gate to source voltage is always at or above its threshold when the load draws near zero current so that very little additional gate charge is required to turn it on more fully.

2. The transconductance power amplifier for amplifying a signal to a capacitive load recited in Claim 1 further comprising means for reducing current to said first N-channel enhancement MOSFET transistor when said power amplifier sinks current from the load through said second N-channel enhancement MOSFET transistor.

3. A transconductance power amplifier for amplifying a signal to a capacitive load, comprising:

a first N-channel enhancement MOSFET transistor operatively arranged to source current to said capacitive load;

a second N-channel enhancement MOSFET transistor operatively arranged to sink current to said capacitive load;

an operational amplifier operatively arranged to transmit and amplify an input signal to both of said first and second MOSFET transistors; and,

means for reducing current to said first N-channel enhancement MOSFET transistor when said power amplifier sinks current from the load through said second N-channel enhancement MOSFET transistor.

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